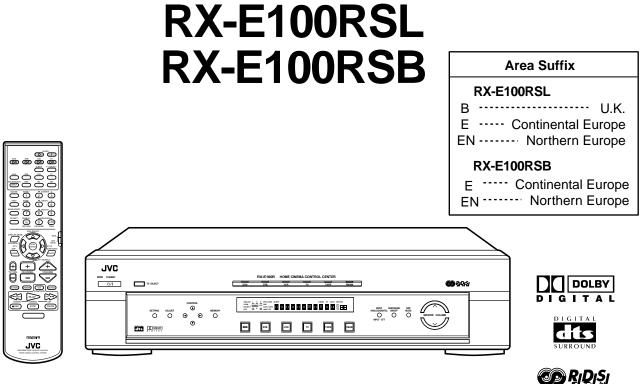
JVC SERVICE MANUAL

AUDIO/VIDEO CONTROL RECEIVER



Each difference points

| MODEL | Source indication lens colour |
|------------|-------------------------------|
| RX-E100RSL | SILVER |
| RX-E100RSB | SILVER BLACK |

Contents

| Safety precautions | 1-2 |
|--------------------------|-----------------|
| Disassembly method | 1- 3 |
| Adjustment method | 1- 8 |
| Description of major ICs | 1-9 ~ 15 |

-Safety Precautions

- 1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
- 2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer's warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
- 3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (A) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
- 4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
- 5. Leakage currnet check (Electrical shock hazard testing)

After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.

Do not use a line isolation transformer during this check.

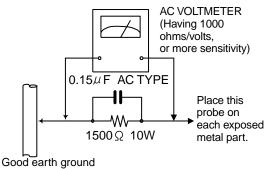
Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).

Alternate check method

Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500 Ω 10W resistor paralleled by a 0.15 μ F AC-type capacitor

between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.

Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

- 1. This equipment has been designed and manufactured to meet international safety standards.
- 2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
- 3. Repairs must be made in accordance with the relevant safety standards.
- 4. It is essential that safety critical components are replaced by approved parts.
- 5. If mains voltage selector is provided, check setting for local voltage.

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (--), diode (+-) and ICP (-) or identified by the " $\underline{\wedge}$ " mark nearby are critical for safety.

When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the JC version)

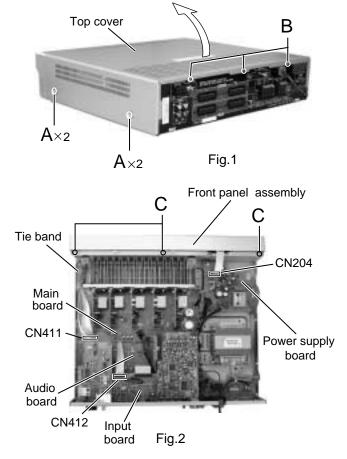
Disassembly method

Removing the top cover (See Fig.1)

- 1. Remove the four screws A attaching the top cover on both sides of the body.
- 2. Remove the three screws B on the back of the body.
- 3. Remove the top cover from behind in the direction of the arrow while pulling both sides outward.

Removing the front panel assembly (See Fig.2 and 3)

- Prior to performing the following procedure, remove the top cover.
- 1. Disconnect the card wire from connector CN411 on the audio board, CN412 on the input board and CN204 on the power supply board in the front panel assembly.
- 2. Cut off the tie band fixing the harness.
- 3. Remove the three screws C attaching the front panel assembly.
- 4. Remove the four screws D attaching the front panel assembly on the bottom of the body. Detach the front panel assembly toward the front.



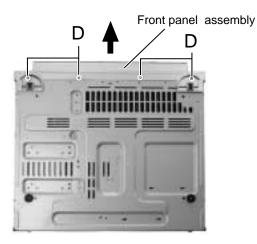


Fig.3

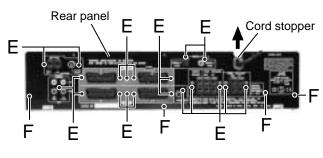


Fig.4

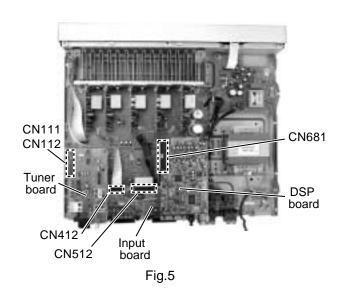
Removing the rear panel (See Fig.4)

- Prior to performing the following procedure, remove the top cover.
- 1. Remove the power cord stopper from the rear panel by moving it in the direction of the arrow.
- 2. Remove the twenty one screws E attaching the each boards to the rear panel on the back of the body.
- 3.

Remove the four screws F attaching the rear panel on the back of the body.

Removing each board connected to the rear side of the audio board (See Fig 5 to 7)

- (See Fig.5 to 7)
- Prior to performing the following procedure, remove the top cover and the rear panel.
- 1. Cut off the tie band fixing the harness.
- 2. Disconnect the tuner board and DSP board from connector CN111,CN112 and CN681 on the each Relay board.
- 3. Disconnect the Relay board from connector CN503, CN504 and CN501 on the audio board.
- 4. Disconnect the card wire connected to connector CN412 and CN512 on the Input board.



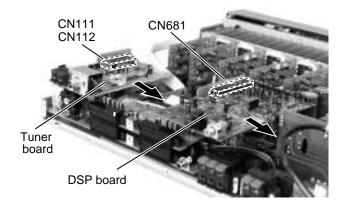
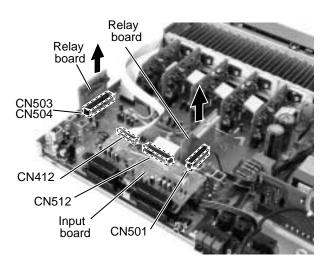


Fig.6





RX-E100RSL/RX-E100RSB

Removing the audio board (See Fig.8)

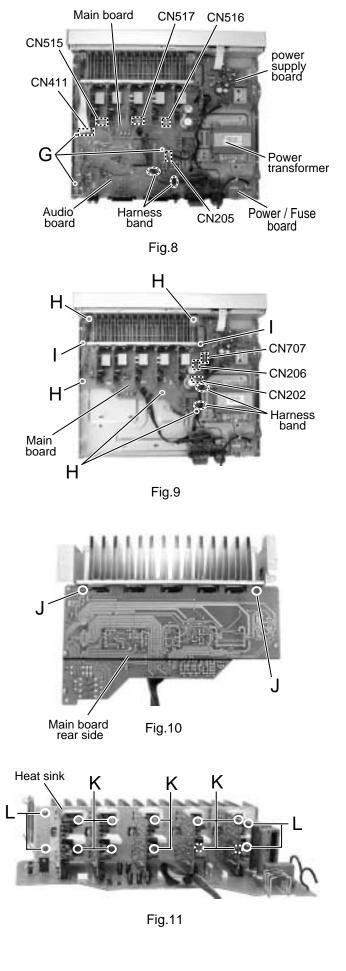
- Prior to performing the following procedure, remove the top cover, the rear panel and the each board.
- 1. Disconnect the card wire from connector CN411 on the audio board.
- 2. Disconnect the harness from connector CN205 on the audio board.
- 3. Disconnect the harness from connector CN515, CN516, and CN517on the main board.
- 4. Remove the harness band fixing the harness.
- 5. Remove the three screws G attaching the audio board assembly.

■ Removing the main board (See Fig.9)

- Prior to performing the following procedure, remove the top cover, the rear panel and audio board.
- 1. Remove the harness band fixing the harness.
- 2. Disconnect the harness from connector CN707 on the power supply board .
- 3. Disconnect the harness from connector CN202 and CN206 on the main board .
- 4. Remove the five screws H and the two screws I attaching the main board.

Removing the Heat sink (See Fig.10 to 11)

- 1. Remove the ten screws K and four screws L attaching the heat sink.
- 2. Remove the two screws J attaching the heat sink from the rear side of main board.



Removing the power supply board (See Fig.12)

- Prior to performing the following procedure, remove the top cover.
- 1. Disconnect the card wire from connector CN204 on the power supply board.
- 2. Disconnect the harness connected to connector CN201 and CN707 on the power supply board (If necessary, cut off the band fixing the harness on the side of the base chassis).
- 3. Disconnect the harness connected to connector CN206 on the main board
- 4. Remove the three screws N attaching the power supply board.
- 5. Unsolder the three harnesses connected to the power supply board.

Removing the power transformer (See Fig.12 and 13)

- Prior to performing the following procedures, remove the top cover.
- 1. Disconnect the harness from connector CN217 on the power / fuse board.
- 2. Disconnect the harness from connector CN201 and CN202 on the power supply board and main board.
- 3. Remove the four screws M attaching the power transformer.

■Removing the power / fuse board

(See Fig.13)

- Prior to performing the following procedure, remove the top cover and the rear panel.
- 1. Disconnect the harness connected to connector CN217 on the power / fuse board (If necessary, cut off the band fixing the harness on the side of the base chassis).
- 2. Unsolder the power cord and other harnesses connected to the power / fuse board.
- 3. Remove the screw O attaching the power / fuse board.

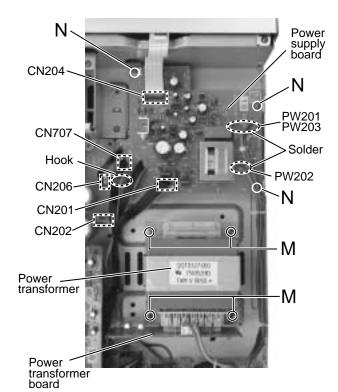
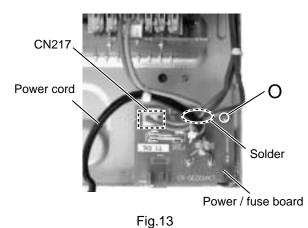


Fig.12



Removing the system control board / power switch board (See Fig.14)

- Prior to performing the following procedure, remove the top cover and the front panel assembly.
- 1. Remove the two screws P attaching the power switch board.
- 2. Remove the eight screws Q attaching the system control board.

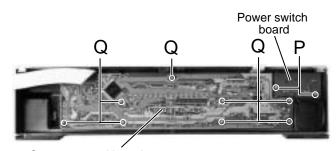


Fig.14

System control board

Adjustment method

Power amplifier section

Adjustment of idling current

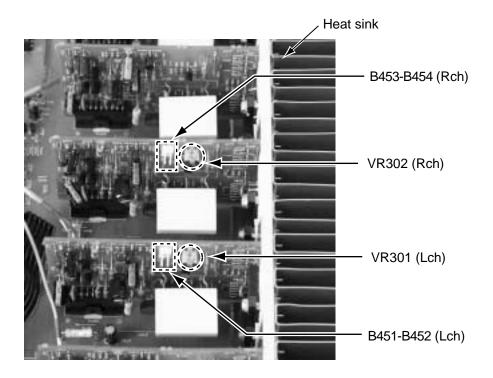
Measurement terminal B451-B452(Lch) , B453-B454(Rch) Adjustment volume VR301(Lch) , VR302(Rch)

Attention

This adjustment does not obtain a correct adjustment value immediately after the amplifier is used (state that an internal temperature has risen). Please adjust immediately after using the amplifier after turning off the power supply of the amplifier and falling an internal temperature.

<Adjustment method>

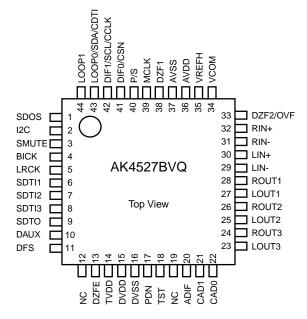
- 1. Prior to turning the power ON, fully turn the adjusting resistor (VR301(Lch),VR302(Rch)) counterclockwise direction and connect the DC voltmeter to the measuring terminal(B451-B452(Lch), B453-B454(Rch)).
- 2. Set the surround mode OFF.
- 3. Adjust the resistor so that the measured value becomes 2mV immediately after turning the power ON.
- 4. When the idling current has been stable (about 30 minutes after the power is turned ON), confirm that the measured value falls within 1.0mV~10mV(2.3mV).
- * It is not abnormal though the idling current might not become 0mA even if it is finished to turn variable resistance (VR301VR302) in the direction of counterclockwise.



Description of major ICs

AK4527B (IC601) : A/D,D/A Converter

1.Pin layout



2. Pin function (1/2)

| 2. Pin 1 | function (1/2 |) | AK4527(1/2) |
|----------|---------------|-----|--|
| No. | Pin name | I/O | Function |
| 1 | SDOS | - | SDTO Source Select Pin (Note 1) |
| | | | "L" : Internal ADC output, "H" : DAUX input |
| 2 | I2C | Ι | Control Mode Select Pin |
| | | | "L" : 3-wire Serial, "H" : I2C Bus |
| 3 | SMUTE | Ι | Soft Mute Pin (Note 1) |
| | | | When this pin goes to "H", soft mute cycle is initialized. |
| | | | When returning to "L", the output mute releases. |
| 4 | BICK | | Audio Serial Data Clock Pin |
| 5 | LRCK | I/O | Input Channel Clock Pin |
| 6 | SDTI1 | Ι | DAC1 Audio Serial Data Input Pin |
| 7 | SDTI2 | Ι | DAC2 Audio Serial Data Input Pin |
| 8 | SDTI3 | Ι | DAC3 Audio Serial Data Input Pin |
| 9 | SDTO | 0 | Audio Serial Data Output Pin |
| 10 | DAUX | - | Sub Audio Serial Data Input Pin |
| 11 | DFS | Ι | Double Speed Sampling Mode Pin (Note 1) |
| | | | "L" : Normal Speed, "H" : Double Speed |
| 12 | NC | - | No Connect |
| | | | No internal bonding. |
| 13 | DZEF | Ι | Zero Input Detect Enable Pin |
| | | | "L" : mode 7 (disable) at parallel mode, |
| | | | zero detect mode is selectable by DZFM2-0 bits at serial mode. |
| | | | "H" : mode 0 (DZF is AND of all six channels) |
| 14 | TVDD | - | Output Buffer Power supply Pin, 2.7V~5.5V |
| 15 | DVDD | - | Digital Power Supply Pin, 4.5V~5.5V |
| 16 | DVSS | - | De-emphasis Pin, 0V |
| 17 | PDN | Ι | Power-Down & Reset Pin |
| | | | When "L", the AK4527B is powered-down and the control registers are reset to default |
| | | | state. If the state of P/S or CAD0-1 changes, then the AK4527B must be reset by PDN. |
| 18 | TST | Ι | Test Pin |
| | | | This pin should be connected to DVSS. |

| Pin fu | Inction (2/2) | | AK4527(1/2) | |
|--------|---------------|-----|---|--|
| No. | Pin name | I/O | No Connect Function | |
| 19 | NC | - | No internal bonding. | |
| | | | Analog Input Format Select Pin | |
| 20 | ADIF | Ι | "H" : Full-differential input, "L" : Single-ended input | |
| | | | Chip Address 1 Pin | |
| 21 | CAD1 | | Chip Address 0 Pin | |
| 22 | CAD0 | | DAC3 Lch Analog Output Pin | |
| 23 | LOUT3 | 0 | DAC3 Rch Analog Output Pin | |
| 24 | ROUT3 | 0 | DAC2 Lch Analog Output Pin | |
| 25 | LOUT2 | 0 | DAC2 Rch Analog Output Pin | |
| 26 | ROUT2 | 0 | DAC1 Lch Analog Output Pin | |
| 27 | LOUT1 | 0 | DAC1 Rch Analog Output Pin | |
| 28 | ROUT1 | 0 | Lch Analog Negative Input Pin | |
| 29 | LIN- | Ι | Lch Analog Positive Input Pin | |
| 30 | LIN+ | Ι | Rch Analog Negative Input Pin | |
| 31 | RIN- | | Rch Analog Positive Input Pin | |
| 32 | RIN+ | I | Zero Input Detect 2 Pin (Note 2) | |
| 33 | DZF2 | 0 | When the input data of the group 1 follow total 8192LRCK cycles with "0" input data, | |
| | | | this pin goes to "H". | |
| | | | Analog Input Overflow Detect Pin (Note 3) | |
| | OVF | 0 | This pin goes to "H" if the analog input of Lch or Rch is overflows. | |
| | | | Common Voltage Output Pin, AVDD/2 | |
| 34 | VCOM | 0 | Large external capacitor around 2.2uF is used to reduce power-supply noise. | |
| | | | Positive Voltage Reference Input Pin,AVDD | |
| 35 | VREFH | - | Analog Power Supply Pin,4.5V~5.5V | |
| 36 | AVDD | - | Analog Ground Pin,0V | |
| 37 | AVSS | - | Zero Input Detect 1 Pin (Note 2) | |
| 38 | DZF1 | 0 | When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, | |
| | | | this pin goes to "H". | |
| | | | Master Clock Input Pin | |
| 39 | MCLK | | Parallel / Serial Select Pin | |
| 40 | P/S | I | "L" : Serial control mode, "H" : Parallel control mode | |
| | | | Audio Data Interface Format 0 Pin in parallel mode | |
| 41 | DIF0 | | Chip select pin in 3-wire serial control mode | |
| | CSN | I | This pin should be connected to DVDD at I2C bus control mode | |
| | | | Audio Data Interface Format 1 Pin in parallel mode | |
| 42 | DIF1 | | Control Data Clock Pin in serial control mode | |
| | SCL/CCLK | I | I2C = "L" : CCLK(3-wire Serial), I2C = "H" : SCL(I2CBus) | |
| | | | Loopback Mode 0 Pin in parallel control mode | |
| 43 | LOOP0 | I | Enables digital loop-back from ADC to 3 DACs. | |
| | | | Control Data Input Pin in serial control mode | |
| | SAD/CDTI | I/O | I2C = "L" : CDTI(3-wire Serial), I2C = "H" : SDA(I2CBus) | |
| | | | Loopback Mode 1 Pin (Note 1) | |
| 44 | LOOP1 | Ι | Enable all 3 DAC channels to be input from SDTII. | |
| | | | | |
| - | • | | | |

Notes : 1. SDOS, SMUTE, DFS, and LOOP1 pins are ORed with register data if P/S = "L".

- 2. The group 1 and 2 can be selected by DZFM2-0 bit if P/S = "L" and DZFME = "L".
- 3. This pin becomes OVF pin if OVFE bit is set to "1" at serial control mode.
- 4. All input pins should not be left floating.

■ UPD784215AGC103 (IC671) : UNIT CPU 1.Pin layout

| ۰. | | | | | | |
|----|-----|----|---|----|----|--|
| | | 75 | ~ | 51 | | |
| | 76 | | | | 50 | |
| | , | | | | | |
| | ć | | | | l | |
| | 100 | | | | 26 | |
| | | 1 | ~ | 25 | | |

2.Pin function

| Pin No. | Symbol | I/O | Function | |
|----------|---------------|----------|---|--|
| 1~8 | - | - | Non connect | |
| 9 | VDD | <u> </u> | Power supply terminal | |
| 10 | X2 | 0 | Connecting the crystal oscillator for system main clock | |
| 11 | X1 | | Connecting the crystal oscillator for system main clock | |
| 12 | VSS | - | Connect to GND | |
| 13 | XT2 | 0 | Connecting the crystal oscillator for system sub clock | |
| 14 | XT2 XT1 | | Connecting the crystal oscillator for system sub clock | |
| 15 | RESET | | System reset signal input | |
| 16 | AUTODATA | | Output of DSP to general-purpose port | |
| 17 | LOCK | | Output of DSP to general-purpose port | |
| 18 | DIGITALO | | Output of DSP to general-purpose port | |
| 19 | FORMAT | | Output of DSP to general-purpose port | |
| 20 | CHANNEL | | Output of DSP to general-purpose port | |
| 20 | | | Output of DSP to general-purpose port | |
| 21 | ERR RSTDET | | Reset signal input | |
| | | | | |
| 23 24 | AVDD | - | Power supply terminal Connect to GND | |
| | AVREF0 | - | | |
| 25~32 | 4)/00 | | Connect to GND | |
| 33 | AVSS | - | Connect to GND | |
| 34,35 | | - | Non connect | |
| 36 | AV REF1 | - | Power supply terminal | |
| 37,38 | RX,TX | - | Not use | |
| 39 | | - | Non connect | |
| 40 | DSPCOM | | Communication port from IC701 | |
| 41 | DSPSTS | 0 | Status communication port to IC701 | |
| 42 | DSPCLK | | Clock input from IC701 | |
| 43 | DSPRDY | | Ready signal input from IC701 | |
| 44 | | - | Non connect | |
| 45,46 | MIDIO_IN/OUT | 1/0 | Interface I/O terminal with microcomputer | |
| 47 | MICK | 0 | Interface I/O terminal with microcomputer of clock signal | |
| 48 | MICS | 0 | Interface I/O terminal with microcomputer of chip select | |
| 49 | MILP | 0 | Interface I/O termonal with microcomputer | |
| 50 | MIACK | 0 | Interface I/O termonal with microcomputer | |
| 51,52 | | - | Non connect | |
| 53 | DSPRST | 0 | Reset signal output of DSP | |
| 54~63 | | - | Non connect | |
| 64,65 | CDTI/CDTO | I/O | Interface I/O terminal with microcomputer | |
| 66 | CCLK | 0 | Interface I/O terminal with microcomputer of clock signal | |
| 67 | CS | 0 | Interface I/O terminal with microcomputer of chip select | |
| 68 | XTS | 0 | OSC Select | |
| 69,70 | | - | Non connect | |
| 71 | PD | 0 | Reset signal output | |
| 72 | GND | - | Connect to GND | |
| 73~80 | | - | Non connect | |
| 81 | VDD | - | Power supply | |
| 82 | 3D-ON | - | Non connect | |
| 83 | 3D-ON | 0 | Switch at output destination of surround channel | |
| 84 | ANA/T-TONE | 0 | Test tone control | |
| 85 | REF-MIX | 0 | Control at output destination of LFE channel | |
| 86 | | - | Non connect | |
| 87 | D.MUTE | 0 | Mute of the digital out terminal is controlled | |
| 88 | S.MUTE | 0 | Mute of the audio signal is controlled | |
| 89 | | - | Non connect | |
| 90~93 | ASW1~4 | 0 | Selection of digital input selector | |
| 94 | TEST | - | Test terminal | |
| 95~100 | | - | Non connect | |
| | | 1 | · · · · · · · · · · · · · · · · · · · | |

■ TC9446F-014 (IC631) : Digital signal processor for dolby digital (AC-3) / MPEG2 audio decode

| Pin No. | Symbol | I/O | Function |
|--------------------|--------------------|-----|---|
| 1 | RST | 1 | Reset signal input terminal (L:reset H:Operation usually) |
| 2 | MIMD | | Microcomputer interface mode selection input terminal (Liserial H:IC bus) |
| 3 | MICS | | Microcomputer interface chip select input terminal |
| 4 | MILP | 1 | Microcomputer interface latch pulse input |
| 5 | MIDIO | I/O | Microcomputer interface data I/O terminal |
| 6 | MICK | 1 | Microcomputer interface clock input terminal |
| 7 | MIACK | Ö | Microcomputer interface acknowledge output terminal |
| 8~11 | FI0~3 | 1 | Flag input terminal 0~3 |
| 12 | IRQ | | Interrupt input terminal |
| 13 | VSS | - | Digital ground terminal |
| 14 | LRCKA | | Audio interface LR clock input terminal A |
| 15 | BCKA | 1 | Audio interface bit clock input terminal A |
| 16~18 | SDO0~2 | 0 | Audio interface data output terminal 0 |
| 19 | SD03 | - | Non connect |
| 20 | LRCKB | 1 | Audio interface LR clock input terminal B |
| 21 | BCKB | I | Audio interface bit clock input terminal B |
| 22 | SDT0 | I | Audio interface data input terminal 0 |
| 23 | SDT1 | I | Audio interface data input terminal 1 |
| 24 | VDD | - | Power supply for digital circuit |
| 25 | LRCKOA | 0 | Audio interface LR clock output terminal A |
| 26 | BCKOA | 0 | Audio interface bit clock output terminal A |
| 27,28 | TEST0,1 | 1 | Test input terminal 0/1 (L:test H:operation usually) |
| 29~31 | LRCKOB, BCKOB, TXO | - | Non connect |
| 32,33 | TEST2,3 | I | Test input terminal (L:test H:operation usually) |
| 34 | RX | 1 | SPDIF input terminal |
| 35 | VSS | - | Ground terminal for digital circuit |
| 36 | TSTSUBO | | Test sub input terminal 0 (L:test H:operation usually) |
| 37 | FCONT | 0 | VCO Frequency control output terminal |
| 38,39 | TSTSUB1,TSTSUB2 | I | Test sub input terminal 1,2 (L:test H:operation usually) |
| 40 | PDO | 0 | Phase error signal output terminal |
| 41 | VDDA | - | Power supply for analog circuit |
| 42 | PLON | I | Clock selection input terminal (L:external clock H:VCO clock) |
| 43 | AMPI | I | AMP.input terminal for LPF |
| 44 | AMPO | 0 | AMP.output terminal for LPF |
| 45 | СКІ | I | External clock input terminal |
| 46 | VSSA | - | Ground terminal for analog circuit |
| 47 | СКО | 0 | DIR Clock output terminal |
| 48 | LOCK | 0 | VCO Lock detection output terminal |
| 49 | VSS | - | Ground terminal for digital circuit |
| 50 | WR | 0 | External SRAM writing signal output terminal |
| 51 | OE | 0 | External SRAM output enable signal output terminal |
| 52 | CE | 0 | External SRAM chip enable signal output terminal |
| 53 | VDD | - | Power supply terminal for digital circuit |
| 54~61 | 107~0 | I/O | External SRAM data I/O terminal 7~0 |
| 62 | VSS | - | Ground terminal for digital circuit |
| 63~70 | AD0~7 | 0 | External SRAM address output terminal 0~7 |
| 71 | VDD | - | Power supply terminal for digital circuit |
| 72~80 | AD8~16 | 0 | External SRAM address output terminal 8~16 |
| 81 | VSS | - | Ground terminal for digital circuit |
| 82~89 | PO0~7 | 0 | General purpose output terminal 0~7 |
| 90 | VDDDL | - | Power supply terminal for DLL |
| 91 | LPFO | 0 | LPF output terminal for DLL |
| 92,93 | DLON,DLCKS | | Refer to the undermentioned table |
| 94 | SCKO | - | Non connect |
| 95 | VSSDL | - | Ground terminal for DLL |
| 96 | SCKI | I | External system clock input terminal |
| | VSSX | - | Ground termonal for oscillation circuit |
| 97 | | | |
| 97 98,99 100 | XO,XI VDDX | I/O | Oscillation I/O terminal Power supply terminal for oscillation circuit |

| DLCKS terminal | DLONterminal | DLL clock setting |
|----------------|--------------|------------------------------|
| L | L | SCKI input (DLL circuit OFF) |
| L | Н | Four times XI clock |
| Н | L | Three times XI clock |
| Н | H | Six times XI clock |

32 VDD

31 🗖 A15 30 CS2

29 🗖 🛛 WE

28 A13 27 A8 26 A9 25 A11

24 🗖 🖻

23 A10

22 Allo 22 CS2 21 I/08 20 I/07 19 I/06

18 1/05

17 1/04

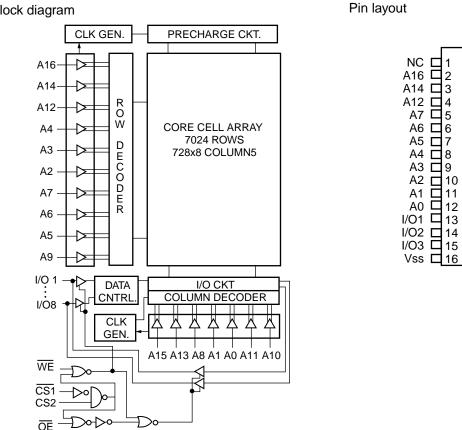
1

4

5

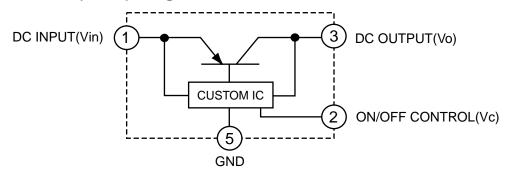
6

■ W24L010AJ-12 (IC641) : CMOS SRAM

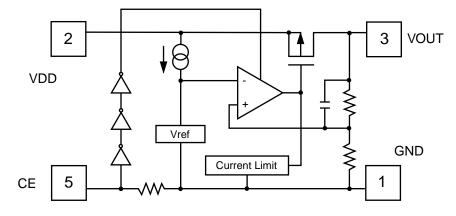


Block diagram

■ PQ3DZ53 (IC681) : Regulator IC



RN5RZ33BA (IC683) : Voltage regurator



RX-E100RSL/RX-E100RSB

MN101C35DHR (IC401) : System controller

| 10 | 0~ | 76 | |
|----|----|----|--|
| 1 | | 75 | |
| ٢ | | ł | |
| 25 | | 51 | |
| 20 | 6~ | 50 | |

Pin function (1/2)

| Pin No. | Symbol | I/O | Function | | |
|---------|---------------|-----|---------------------|--|--|
| 1 | TXD/SB00/P00 | - | GND | | |
| 2 | RXD/SBI0/P01 | - | GND | | |
| 3 | SBT0/P02 | I | PROTECTOR INPUT | | |
| 4 | SB01/P03 | - | GND | | |
| 5 | SBI1/P04 | - | GND | | |
| 6 | SBT1/P05 | I | GND (TV LINK INPUT) | | |
| 7 | BUZZER/P06 | I | SLOW SW L INPUT | | |
| 8 | VDD | - | POWER SUPPLY +5V | | |
| 9,10 | OSC1,2 | I/O | OSC (8MHz) | | |
| 11 | VSS | - | GND | | |
| 12 | XI | - | GND | | |
| 13 | X0 | 0 | OPEN | | |
| 14 | MMOD | - | GND | | |
| 15 | VREF- | - | GND | | |
| 16 | AN0/PA0 | I | KEY INPUT 1 (7KEY) | | |
| 17 | AN1/PA1 | I | KEY INPUT 2 (7KEY) | | |
| 18 | AN2/PA2 | I | KEY INPUT 3 (7KEY) | | |
| 19 | AN3/PA3 | I | CHIP SELECT 1 | | |
| 20 | AN4/PA4 | I | CHIP SELECT 2 | | |
| 21 | AN5/PA5 | I | SCART DVD INPUT | | |
| 22 | AN6/PA6 | I | SCART STB INPUT | | |
| 23 | AN7/PA7 | I | SCART VCR INPUT | | |
| 24 | VREF+ | - | POWER SUPPLY +5V | | |
| 25 | P07 | 0 | SLOW SW M OUTPUT | | |
| 26 | RST /P27 | | RESET INPUT | | |
| 27 | TM0IO/P10 | 0 | RDS SDA IN/OUT | | |
| 28 | TM1IO/P11 | | RDS SCL IN/OUT | | |
| 29 | TM2IO/P12 | 0 | TUNER CE | | |
| 30 | TM3IO/P13 | I | TUNER MUTE | | |
| 31 | TM4IO/P14 | 0 | TUNER CLK | | |
| 32 | P15 | I/O | TUNER DATA IN/OUT | | |
| 33 | IRQ0/P20 | - | GND | | |
| 34 | SENS/IRQ1/P21 | I | REMOCON INPUT | | |
| 35 | IRQ2/P22 | I | INH INPUT | | |
| 36 | IRQ3/P23 | | RDS DAVN INPUT | | |
| 37 | IRQ4/P24 | I | TUNED INPUT | | |
| 38 | P25 | I | STEREO INPUT | | |
| 39 | SB02/P30 | 0 | DSP MICON COMMAND | | |
| 40 | SBI2/P31 | I | DSP MICON STATUS | | |

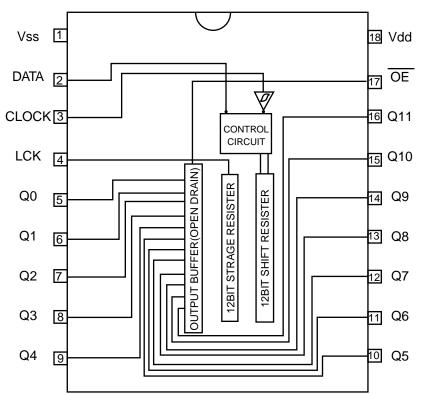
Pin function (2/2)

| Pin No. | Symbol | I/O | Function |
|-----------------|-----------------|--------------|-----------------------|
| 41 | SBT2/P32 | 0 | DSP MICON CLK |
| 42 | P50 | 0 | DSP MICON READY |
| 43 | P51 | 0 | DSP MICON RESET |
| 44 | P52 | 0 | M61501 CLK |
| 45 | P53 | 0 | M61501 DATA |
| 46 | P54 | 0 | M61501 LATCH |
| 47 \$ | DGT17/P67 | 0 | VIDEO SELECT 1 |
| 50 | DGT14/P64 | 0 | VIDEO SELECT 4 |
| 51 | DGT13/P63 | 0 | GRID 1 |
| 51 \$ 54 | DGT10/P60 | 0 | GRID 4 |
| 55 | DGT9/P41 | 0 | GRID 5 |
| 56 | DGT8/P40 | 0 | GRID 6 |
| 57 \$ | SEG0/DGT7/P77 | - | GRID 7 |
| 63 | SEG6/DGT1/P71 | 0 | GRID 13 |
| 64 | SEG7/DGY0/P7 | O SEGMENT 17 | |
| 65 | SEG8/P87 | - | SEGMENT 18 |
| 5 72 | \$ SEG15/P80 | 0 | SEGMENT 25 |
| 73 | SEG16/P97 | | SEGMENT 1 |
| \$ 88 | SEG31/PB3 | 0 | SEGMENT 16 |
| 89 | SEG32/PB2 | 0 | STANDBY LED |
| 90 | SEG33/PB1 | 0 | EXPANSION BU2092 LCK |
| 91 | SEG34/PB0 | 0 | EXPANSION BU2092 DATA |
| 92 | SEG35/PD7 | 0 | EXPANSION BU2092 CLK |
| 93 | SEG36/PD6 | 0 | FRONT SPK RELAY |
| 94 | SEG37/PD5 | 0 | CENTER SPK RELAY |
| 95 | SEG38/PD4 | 0 | REAR SPK RELAY |
| 96 | SEG39/PD3 | 0 | POWER ON |
| 97 | SEG40/PD2 | 0 | SWITCH MODE ON |
| 98 | SEG41/PD1 | 0 | SUBWFR MUTE |
| 99 | SEG42/PD0 | 0 | SOURCE MUTE |
| 100 | VPP | 0 | VPP |

RX-E100RSL/RX-E100RSB

BU2092 (IC642) : Port expander

1.Terminal Layout

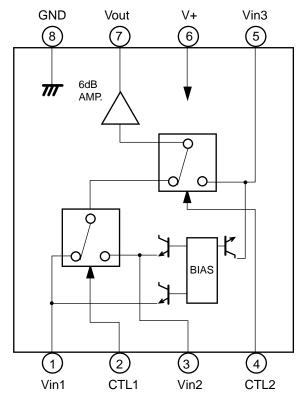


2.Pin Function

| Pin No. | Symbol | I/O | Function |
|---------|--------|-----|---|
| 1 | Vss | - | Connect to GND |
| 2 | DATA | Ι | Serial Data input |
| 3 | CLOCK | I | Shift Clock of Data |
| 4 | LCK | Ι | Latch Clock of Data |
| 5~16 | Q0~Q11 | 0 | Parallel Data Output Latch Data L H OUTPUT ON OFF |
| 17 | OE | I | Output Enable |
| 18 | Vdd | - | Power Supply |

■ NJM2246M (IC511,IC512,IC513) : Video switch

Block diaglam

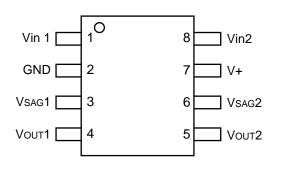


INPUT CONTROL SIGNAL- OUTPUT SIGNAL

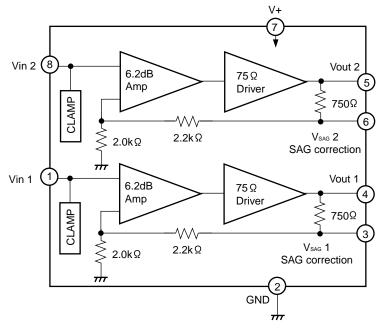
| CTL1 | CTL2 | OUTPUT SIGNAL |
|------|------|---------------|
| L | L | Vin1 |
| Н | L | Vin2 |
| L/ H | Н | Vin3 |

■ NJM2267M (IC516) : Video switch

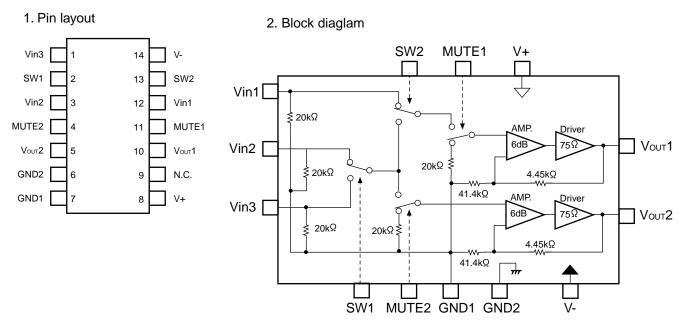
1. Pin layout



2. Block diaglam



■ NJM2279M (IC515) : Video switch



■ NJM2293 (IC514) : Video switch

Block diaglam

